Call for papers -- Special Session on:
Tools and Design of Embedded on chip communications and systems
for CODIT2014
November 3-5, 2014 - Metz, France

Session chair
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Session description
The field of embedded system is getting more and more challenging, and issues in development of embedded hardware are becoming very attracting to a wide number of researchers both in industry and academia. Thus, On-chip parallel, reconfigurable and network-based system design to achieve functionality with constraints product requires design methodology, architectures, energy and performance evaluation schemes. Such systems, which are emerging as the architecture of choice for future high performance embedded hardware systems, processors or reconfigurable systems, require high performance interconnects, new paradigms and architecture mechanisms which are necessary to satisfy all constraints and embedded applications. This session is dedicated to research both practical and theoretical issues in the development of embedded systems, especially operating on reconfigurable technology (i.e. FPGA), on embedded on-chip communication and system, architecture, design methods and applications, bringing together scientists and engineers working on on-chip innovations from related research communities, including parallel computer architecture, CAD and verification tools, networking and embedded multi-processor systems. Major topics of interest include but are not limited to the following:
Topics
- *System and communication on-chip (SoC, MPSoC, NoC) design methodologies, platforms and applications*
- *SoC and NoC design methodologies and tools, Silicon and Logic optimization*
- *Reconfigurable computing, system design, synthesis and optimization*
- *Embedded networked systems and software, Modelling and Simulation*
- *Design for testability, Testing and Formal verification, debug and test of NoCs and SoCs*
- *Memory system design and optimizations for SoCs*
- *On-chip network architecture and reliability for FPGAs and structured ASICs, Network design for 3D stacked logic and memory, Mapping of applications onto NoCs*
- *High level synthesis tools and CAD for FPGAs*

Submission
Please submit your full paper or extended abstract of 2 to 3 pages choosing the right track on the Easychair site:
https://www.easychair.org/conferences/?conf=codit14
June 20, 2014: deadline for paper submission
July 10, 2014: notification of acceptance/reject
September 10, 2014: deadline for final paper and registration.

http://codit2014.event.univ-lorraine.fr/